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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/608,286	06/27/2003	Abbas Ali	TI-31505A	8530

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EXAMINER

VINH, LAN

ART UNIT	PAPER NUMBER
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1765

DATE MAILED: 07/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/608,286

Applicant(s)

ALI ET AL.

Examiner

Lan Vinh

Art Unit

1765

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 06 June 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-12 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 3, 6 are rejected under 35 U.S.C. 102(e) as being anticipated by Flanner et al (US 6,410,437)

Flanner discloses a process for manufacturing dual damascene. This process comprises the steps of:

providing a silicon substrate 16 containing conductive line 18 (col 5, lines 8-10; fig. 3), which reads on providing a silicon substrate containing one or more electronic devices

forming a first dielectric layer 12 (OSG) over the substrate 16, layer 12 having a thickness/first thickness (col 5, lines 54-55; fig. 3)

forming a first etch stop layer 10 (SiN) over dielectric layer 12/first dielectric layer (col 5, lines 1-5; fig. 3)

forming a second dielectric layer 8 over the first dielectric layer 12, layer 8 having a thickness (col 5, lines 20-25, fig. 3)

forming an antireflective coating/ARC layer 4 over dielectric layer 8/second dielectric, the layer 4 is formed prior to the etching step to form the trench (col 5, lines 33-35 ; fig. 3)

etching a first trench in the dielectric layer 8/second dielectric layer (col 6, lines 53-55; fig.11)

etching at the same time a second trench having a depth in the second dielectric layer 8 and the first trench in the first dielectric layer 12 (col 6, lines 50-55 and fig. 12, fig. 12 shows that the depth of second trench/second depth is approximately equal to the thickness of second dielectric layer 8

forming a liner film in the first and second trench (col 6, lines 63-65)

forming a contacting/conductive copper layer filling both first and second trenches (col 8, lines 27-29))

The limitations of claims 3, 6 have been discussed above

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 2, 7-9, 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Flaner et al (US 6,410,437) in view of Plat (US 6,420,280).

Flanner discloses a process for manufacturing dual damascene. This process comprises the steps of:

providing a silicon substrate 16 containing conductive line 18 (col 5, lines 8-10; fig. 3), which reads on providing a silicon substrate containing one or more electronic devices

forming a first dielectric layer 12 (OSG) over the substrate 16, layer 12 having a thickness/first thickness (col 5, lines 54-55; fig. 3)

forming a first etch stop layer 10 (SiN) over dielectric layer 12/first dielectric layer (col 5, lines 1-5; fig. 3)

forming a second dielectric layer 8 over the first dielectric layer 12, layer 8 having a thickness (col 5, lines 20-25, fig. 3)

forming an antireflective coating/ARC layer 4 over dielectric layer 8/second dielectric, the layer 4 is formed prior to the etching step to form the trench (col 5, lines 33-35 ; fig. 3)

etching a first trench in the dielectric layer 8/second dielectric layer, the trench has a depth that is greater than the thickness of layer 8/second dielectric (col 6, lines 53-55; fig.11)

etching at the same time a second trench having a depth in the second dielectric layer 8 and the first trench in the first dielectric layer 12 (col 6, lines 50-55 and fig. 12, fig. 12 shows that the depth of second trench/second depth is approximately equal to the thickness of second dielectric layer 8

forming a liner film in the first and second trench (col 6, lines 63-65)

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forming a contacting/conductive copper layer filling both first and second trenches
(col 8, lines 27-29)

Unlike the instant claimed inventions as per claims 2, 7, Flanner fails to disclose forming an ARC layer of SiON

Plat discloses a method for forming a semiconductor device comprises the step of forming a SION ARC layer (col 4, lines 39-40)

Hence, one skilled in the art at the time the invention was made would have found it obvious to modify Flanner method by forming an ARC layer of SiON as per Plat because Plat discloses that the conventional ARC layer is typically a SION (col 4, lines 35-37)

Regarding claim 8, one skilled in the art at the time the invention was made would have found it obvious that Flanner and Plat silicon oxynitride ARC layer would have had the atomic percent numbers as recited in claim 8 because the atomic percent numbers are physical properties of SiON (see prior art of record for evidence of this basis)

The limitations of claims 9, 12 have been discussed above

5. Claims 4-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Flanner et al (US 6,410,437) in view of Lin et al (US 6,342,448)

Flaner's method has been described above. Flanner differs from the instant claimed inventions as per claims 4-5 by forming the first and second dielectric layers of OSG instead of FSG (Fluorosilicate glass)

However, Lin, in a method of forming dual damascene, discloses that a dielectric layer can be formed of OSG or FSG (col 4, lines 14-16)

Hence, one skilled in the art would have found it obvious to substitute Flanner OSG dielectric layer with FSG in view of Liu teaching because Lin discloses that the OSG dielectric layer can alternately be formed of FSG (col 4, lines 6-16)

6. Claims 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Flanner et al (US 6,410,437) in view of Plat (6,420,280) and further in view of Lin et al (US 6,342,448)

Flanner as modified by Plat method has been described above. Flanner and Plat differ from the instant claimed inventions as per claims 10-11 by forming the first and second dielectric layers of OSG instead of FSG (Fluorosilicate glass)

However, Lin, in a method of forming dual damascene, discloses that a dielectric layer can be formed of OSG or FSG (col 4, lines 14-16)

Hence, one skilled in the art would have found it obvious to substitute Flanner and Plat OSG dielectric layer with FSG in view of Lin teaching because Liu discloses that the OSG dielectric layer can alternately be formed of FSG (col 4, lines 6-16)

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Sim et al (US 6,423,654) discloses that SiON has an atomic composition ratio of silicon (25-40%), oxygen (25-40%), nitrogen (25-40%) (abstract)

Response to Arguments

8. Applicant's arguments with respect to claims 1-12 have been considered but are moot in view of the new ground(s) of rejection.

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lan Vinh whose telephone number is 571 272 1471. The examiner can normally be reached on M-F 8:30-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on 571 272 1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



LV

July 8, 2005